FORM PTO-1390 (REV. 12-2001) U.S DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY 'S DOCKET NUMBER: 8074-5 (S1595 SB/swi)

U.S. APPLICATION NO. (If known, see 37 CFR 1.5): 10/070126

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/EP00/08598	01 September 2000	02 September 1999

TITLE OF INVENTION
Cell Contention Resoltuion Unit for a Device for Switching a Plurality of Packet-Oriented Signals

APPLICANT(S) FOR DO/EO/US
Mathias Hellwig and Andreas Kirstaedter

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. [X] This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. [ ] This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. [X] This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (21) indicated below.
4. [ ] The US has been elected by the expiration of 19 months from the priority date (Article 31).
5. [X] A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. [X] is attached hereto (required only if not communicated by the International Bureau).
   b. [X] has been communicated by the International Bureau.
   c. [ ] is not required, as the application was filed in the United States Receiving Office (RO/US).
6. [X] An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. [X] is attached hereto.
   b. [ ] has been previously submitted under 35 U.S.C. 154(d)(4).
7. [ ] Amendments to the claims of the International Aplication under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. [ ] are attached hereto (required only if not communicated by the International Bureau).
   b. [ ] have been communicated by the International Bureau.
   c. [ ] have not been made; however, the time limit for making such amendments has NOT expired.
   d. [ ] have not been made and will not be made.
8. [ ] An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371 (c)(3)).
9. [X] An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. [ ] An English lanugage translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11 to 20 below concern document(s) or information included:

11. [ ] An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. [X] An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. [X] A FIRST preliminary amendment.
14. [ ] A SECOND or SUBSEQUENT preliminary amendment.
15. [ ] A substitute specification.
16. [ ] A change of power of attorney and/or address letter.
17. [ ] A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825.
18. [ ] A second copy of the published international application under 35 U.S.C. 154(d)(4).
19. [ ] A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
20. [X] Other items or information: International Search Report, IPER with Annexes

U.S. APPLICATION NO. (if known, see 37 CFR 1.5)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
10/070126	PCT/EP00/08598	8074-5 (S1595 SB/swi)

21. [X] The following fees are submitted:	CALCULATIONS PTO USE ONLY	
BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)):		
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO **$1040.00**		
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO **$890.00**		
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO **$740.00**		
International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) **$710.00**		
International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) **$100.00**		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 890.00	
Surcharge of **$130.00** for furnishing the oath or declaration later than [ ] 20 [ ] 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$ 0	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE	$
Total claims	18 - 20 =	0	x **$18.00**	$ 0
Independent claims	1 - 3 =	0	x **$84.00**	$ 0
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ **$280.00**	$ 0

TOTAL OF ABOVE CALCULATIONS =	$ 890.00	
[ ] Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2. +	$ 0	
SUBTOTAL =	$ 890.00	
Processing fee of **$130.00** for furnishing the English translation later than [ ] 20 [ ] 30 months from the earliest claimed priority date (37 CFR 1.492(f)).	$ 0	
TOTAL NATIONAL FEE =	$ 890.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property +	$ 40.00	
TOTAL FEES ENCLOSED =	$ 930.00	
	Amount to be refunded:	$
	charged:	$

a. [X] A check in the amount of $ 930.00 to cover the above fees is enclosed.

b. [ ] Please charge my Deposit Account No. _____ in the amount of $ _____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. [X] The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 50-0679 . A duplicate copy of this sheet is enclosed.

d. [ ] Fees are to be charged to a credit card. **WARNING:** Information on this form may become public. **Credit card information should not be included on this form.** Provide credit card information and authorization on PTO-2038.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137 (a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

Frank Chau
F. CHAU & ASSOCIATES, LLP
1900 Hempstead Turnpike, Suite 501
East Meadow, New York 11554
(516) 357-0091

SIGNATURE

Frank Chau
NAME

34,136
REGISTRATION NUMBER

Attorney Docket: 8074-5 (S1595 SB/fis)

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT(S): Mathias Hellwig et al.

INT'L. APPLN. NO: PCT/EP00/08598

INT'L. FILING DATE: September 1, 2000

FOR: CELL CONTENTION RESOLUTION UNIT FOR A DEVICE FOR SWITCHING A PLURALITY OF PACKET-ORIENTED SIGNALS

Assistant Commissioner for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Before examination of the above-identified application on the merits, kindly amend the application as follows:

IN THE CLAIMS:

Please cancel claims 1-3, 6-7, 9 and 12-14.

Please accept amended claims 4-5, 8, 10-11 and 15-18 as follows:

CERTIFICATION UNDER 37 C.F.R. § 1.10

I hereby certify that this New Application Transmittal and the documents referred to as enclosed therein are being deposited with the United States Postal Service on this date March 1, 2002 in an envelope as "Express Mail Post Office to Addressee" Mail Label Number EL922712475US addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231.

Frank Chau

4. (Amended) The cell contention resolution unit as claimed in claim 1, in which each availability vector (CRreq) has N bits, the position of a bit in the availability vector (CRreq) comprising the assignment of the information contained in this bit to a particular port unit, and the one logical state of the bit signaling the availability of a packet or a cell intended for the port unit concerned and the other logical state, respectively, signaling the absence of the availability of a packet or a cell.

5. (Amended) The cell contention resolution unit as claimed in claim 1, in which the reservation vector (CRres) has N bits, the position of a bit in the reservation vector (CRres) comprising the assignment of the information contained in this bit to a particular receiving port unit, and the one logical state of the bit signaling the already performed reservation of the port unit concerned for the reception of a packet or a cell from another port unit, and the other logical state, respectively, signaling the readiness of the port unit concerned.

8. (Amended) The cell contention resolution unit as claimed in claim 1, in which each comparator unit ascertains the authorization information for the port unit concerned in a predetermined sequence with respect to the port units or the individual bits of the reservation vector (CRres).

10. (Amended) The cell contention resolution unit as claimed in claim 1, which each comparator unit ascertains a possible reservation of bits of the reservation vector (CRres) in the sequence of the bits of the reservation vector (CRres), in which

each comparator unit is preceded by a permutation unit, to which the availability vector (CRreq) can be fed and which re-orders the bits of the availability vector (CRreq) in their sequence in accordance with a predetermined specification and in which each comparator unit is followed by a inverse permutation unit, which, taking into account the performed permutation of the sequence of the bits of the availability vector (CRreq), ascertains from the information fed to it by the comparator unit, concerning whether and which position of the reservation vector (CRres) has been reserved, which authorization information (CRgnt) is to be transmitted to the port unit connected to the comparator unit concerned.

11. (Amended) The cell contention resolution unit as claimed in claim 1, in which the selection authorization for the transmission of the respective packet or the respective cell to another port unit, respectively, is provided in each comparator unit by N-1 quota counters provided for each of the other N-1 port units, respectively, or by N quota counters provided for each bit of the reservation vector (CRres), the counter reading (quota) of a quota counter being incremented or decremented after each selection of the assigned port unit or after each reservation of the associated bit of the reservation vector (CRres) and, once a predetermined counter reading has been reached, the selection authorization for the port unit concerned or the reservation authorization for the bit concerned of the reservation vector (CRres) being blocked.

15. (Amended) The cell contention resolution unit as claimed in claim 12, in which one or more quota counters are assigned a higher initial quota than other quota counters.

16. (Amended) The cell contention resolution unit as claimed in claim 1, in which the comparator units each have an N-staged priority encoder, each of the N inputs (I_1 to I_N) of the priority encoder being connected to the output of an AND element, and a first input of the AND element being fed the corresponding bit (CRreq[i]) of the availability vector or of the permuted availability vector (CRreq*[i]), a second input of the AND element being fed the bit concerned of the reservation vector (CRres[i]), which lies at the output of the respectively preceding comparator unit, and a third input of the AND element being fed the information of the associated quota counter, which is logical ONE if there is still a selection authorization, and logical ZERO if there is no longer any selection authorization.

17. (Amended) The cell contention resolution unit as claimed in claim 1, which is designed as an integrated circuit.

18. (Amended) A central switching device with N ports for the connection of a maximum of N port units, which is designed as an integrated circuit which comprises a cell contention resolution unit as claimed in one of claim 1.

REMARKS

Before examination on the merits of the above application, please enter the present Preliminary Amendment. Early and favorable reconsideration is respectfully requested.

Respectfully submitted,

By: _____
Frank Chau
Reg. No. 34,136

Mailing Address:
F. Chau & Associates, LLP
1900 Hempstead Turnpike, Suite 501
East Meadow, New York 11554
Tel. No. (516) 357-0091
Fax No. (516) 357-0092

MARKED-UP VERSION OF THE CLAIMS

4. (Amended) The cell contention resolution unit as claimed in [one of the preceding claims] claim 1, in which each availability vector (CRreq) has N bits, the position of a bit in the availability vector (CRreq) comprising the assignment of the information contained in this bit to a particular port unit [(3)], and the one logical state of the bit signaling the availability of a packet or a cell intended for the port unit [(3)] concerned and the other logical state, respectively, signaling the absence of the availability of a packet or a cell.

5. (Amended) The cell contention resolution unit as claimed in [one of the preceding claims] claim 1, in which the reservation vector (CRres) has N bits, the position of a bit in the reservation vector (CRres) comprising the assignment of the information contained in this bit to a particular receiving port unit [(3)], and the one logical state of the bit signaling the already performed reservation of the port unit [(3)] concerned for the reception of a packet or a cell from another port unit [(3)], and the other logical state, respectively, signaling the readiness of the port unit concerned.

8. (Amended) The cell contention resolution unit as claimed in [one of the preceding claims] claim 1, in which each comparator unit [(13)] ascertains the authorization information for the port unit [(3)] concerned in a predetermined sequence with respect to the port units [(3)] or the individual bits of the reservation vector (CRres).

10. (Amended) The cell contention resolution unit as claimed in [one of claims

1 to 8] claim 1, in which each comparator unit [(13)] ascertains a possible reservation of bits of the reservation vector (CRres) in the sequence of the bits of the reservation vector (CRres), in which each comparator unit [(13)] is preceded by a permutation unit [(15)], to which the availability vector (CRreq) can be fed and which re-orders the bits of the availability vector (CRreq) in their sequence in accordance with a predetermined specification and in which each comparator unit [(13)] is followed by a inverse permutation unit [(19)], which, taking into account the performed permutation of the sequence of the bits of the availability vector (CRreq), ascertains from the information fed to it by the comparator unit [(13)], concerning whether and which position of the reservation vector (CRres) has been reserved, which authorization information (CRgnt) is to be transmitted to the port unit [(3)] connected to the comparator unit [(13)] concerned.

11. (Amended) The cell contention resolution unit as claimed in [one of the preceding claims] claim 1, in which the selection authorization for the transmission of the respective packet or the respective cell to another port unit [(3)], respectively, is provided in each comparator unit [(13)] by N-1 quota counters [(21)] provided for each of the other N-1 port units [(3)], respectively, or by N quota counters [(21)] provided for each bit of the reservation vector (CRres), the counter reading (quota) of a quota counter [(21)] being incremented or decremented after each selection of the assigned port unit [(3)] or after each reservation of the associated bit of the reservation vector (CRres) and, once a predetermined counter reading has been reached, the selection authorization for the port unit [(3)] concerned or the reservation authorization for the bit concerned of the reservation vector (CRres) being blocked.

15. (Amended) The cell contention resolution unit as claimed in [one of the claims 12 to 14] claim 12, in which one or more quota counters [(21)] are assigned a higher initial quota than other quota counters [(21)].

16. (Amended) The cell contention resolution unit as claimed in [one of the preceding claims] claim 1, in which the comparator units [(13)] each have an N-staged priority encoder (23), each of the N inputs (I_1 to I_N) of the priority encoder [(23)] being connected to the output of an AND element [(25)], and a first input of the AND element being fed the corresponding bit (CRreq[i]) of the availability vector or of the permuted availability vector (CRreq*[i]), a second input of the AND element [(25)] being fed the bit concerned of the reservation vector (CRres[i]), which lies at the output of the respectively preceding comparator unit [(13)], and a third input of the AND element [(25)] being fed the information of the associated quota counter [(21)], which is logical ONE if there is still a selection authorization, and logical ZERO if there is no longer any selection authorization.

17. (Amended) The cell contention resolution unit as claimed in [one of the preceding claims] claim 1, which is designed as an integrated circuit.

18. (Amended) A central switching device with N ports for the connection of a maximum of N port units [(3)], which is designed as an integrated circuit which comprises a cell contention resolution unit [(8)] as claimed in [one of claims 1 to 14] claim 1.

Description

Cell contention resolution unit for a device for switching a plurality of packet-oriented signals

The invention relates to a cell contention resolution unit for a device for switching a plurality of packet-oriented signals.

In recent years, there has been a great increase in the transmission capacity or the data transmission rate in networks. This has led to the need to develop switching devices, in particular switches and routers, which have a data throughput in the multi-gigabit or even terabit range. At such high transmission speeds, the necessary network protocols can only be produced as hardware.

One option is for switching devices for these high transmission speeds to be produced as an active backplane using a crossbar architecture. Crossbar switching architectures operate entirely in parallel, so that the throughput of such devices is limited only by the number of individual ports and the coordination protocol used internally.

Crossbar architectures usually operate with a plurality of port chips connected to a central crossbar chip by means of interfaces. Known crossbar chips usually contain buffer memories for temporarily storing packets or cells when collisions occur. The cells are produced by segmenting a packet into cells of a particular length (which is a customary procedure - particularly with packets of variable length), which are then processed further within the switching device. This makes it possible to process the cells rationally in sync with the clock. In addition, when collisions occur, i.e. when a plurality of ports of the port chips attempt to transmit to the same port of another port

chip, "fair" transmission of the signals or packets present on the competing ports is facilitated. To this end, a number of known devices with the crossbar chip have an external contention resolution unit (cell contention resolution unit), which uses particular algorithms to ascertain a fair selection of the competing ports.

For example, DE 195 40 160 A1 discloses a method of coordinating input-buffered ATM switching devices via serial lines to avoid output blockages, in which ATM cells competing with respect to an output are already buffered at the input of the corresponding switching device. This switching device comprises in principle a plurality of port chips each with a plurality of ports, the "output ports" of which are interconnected via a crossbar chip. The freedom from blockage of the device is achieved by the use of a reservation vector, the individual bits of which respectively correspond to a (destination) port chip. The reservation vector is passed on successively from port chip to port chip before the transmission of a cell, each port chip having the possibility, in the sequence in which the reservation vector is passed on, to reserve a bit of the reservation vector. If a bit is reserved, this means that the (source) port chip concerned would like to transmit a cell to that (destination) port chip which corresponds to the respective position of the reserved bit of the reservation vector. This (destination) port chip, or this output of the crossbar chip and the respectively reserved bit of the reservation vector, is then no longer available, for the transmission of a cell in the respective time slot, to the next port chip to which the reservation vector is passed on.

In the case of this known device, the processing of the reservation vector takes place in the port chips, the

reservation vector being transmitted between the port chips on a serial connection line.

As a result, external high-speed transmission lines are needed between the portchips to produce the hardware of a switching unit of this type, and this requires corresponding expenditure in terms of design and hardware. Moreover, the reservation vector is passed on from port chip to port chip in a clock-pulse controlled and serial manner, the reservation vector being advanced only by one bit in each clock cycle. In this way, each port unit, which already has one bit of the reservation vector available to it, can in each case only process one bit, preferably the bit just transferred in the respective cycle. If there are N port chips, consequently a total of 2N clock cycles are necessary to process the reservation vector completely. When there are a relatively large number of port chips, this is accompanied by timing problems, since only a very limited time period, which is less than the complete cycle for the transmission of a cell (time slot), is available for this check. Consequently, either the number of port chips is restricted or extremely high clock-pulse rates have to be used in the processing of the reservation vector. This device has a cell contention resolution unit with a decentralized structure, which is accompanied by the disadvantages mentioned.

A fairness balance with respect to competing transmissions to various (destination) port chips can take place in the case of the device according to DE 195 40 160 A1 by the sequence of access to the buffer memories of the individual port chips assigned to each other port chip being changed in each case at the beginning of a complete cycle. This produces, in principle, an altered assignment of the bit positions of the reservation vector to the port chips, so that a

fairness balance is made possible by the altered reservation sequence.

To this end, DE 195 44 920 C2 discloses a method for the fast and fair hardware-based random selection of signals, the total number of all the signals being continually checked for activity in a pseudo-randomly regenerated sequence and, according to a desired number k of signals to be selected, the first k signals found to be active in the test sequence being selected. This method makes a very good fairness balance possible in a simple way.

On the basis of this prior art, the object of the invention is to provide a cell contention resolution unit for a device for switching a plurality of packet-oriented signals with which a switching device can be produced in a simple way and with low expenditure on external hardware, and which is distinguished by a high processing speed in the ascertainment of an adequately fair blockage-free combination of simultaneously possible transmission authorizations between a plurality of ports of a switching device for packet-oriented signals.

The invention achieves this object by the features of patent claim 1.

The invention is based on the finding that an extremely high speed can be achieved in the ascertainment of a blockage-free combination of simultaneously permissible transmission paths between the N ports of a central switching device, while ensuring adequate fairness, by providing a cascade of N comparator units in such a way that a reservation vector is passed through in parallel in the cascade of comparator units, with the processing of the reservation vector, and consequently the generation of the authorization information, in the

comparator units taking place in parallel or semi-parallel.

According to the preferred embodiment of the invention, the processing of the reservation vector in the comparator units and the passing on of the reservation vector between the comparator units takes place in a clock-pulse controlled manner, it also being possible, taking into account signal transit times and switching times of the hardware involved, for the processing of the reservation vector to take place in a plurality of comparator units or all the comparator units in one clock cycle. This allows an extreme increase in the processing speed to be achieved.

In the preferred embodiment, each availability vector which is transferred from one particular port unit in each case to one particular comparator unit in each case has N bits, the position of a bit in the availability vector comprising the assignment of the information contained in this bit to a particular port unit, and the one logical state of the bit signaling whether a packet or a cell which is to be transmitted to that port unit which corresponds to the position of the respective bit in the availability vector is available in the port unit supplying the availability vector, and the other logical state, respectively, signaling the absence of the availability of a packet or a cell. This makes possible a simple selection of packets or cells which can be transmitted simultaneously without blockage.

Although only N-1 bits would be necessary as an availability vector for each port unit, this would have the consequence that processing would be made more difficult by the different assignment in each case of the bits to the (receiving) port units.

In the same way, in the case of the preferred embodiment, the reservation vector also comprises N bits, the position of a bit in the reservation vector comprising the assignment of the information contained in this bit to a particular port unit, and the one logical state of the bit signaling the already performed reservation of the port unit concerned for the reception of a packet or a cell from another port unit, and the other logical state, respectively, signaling the readiness of the port unit concerned.

The control unit transmits at the beginning of a processing cycle an initial reservation vector to the first comparator unit in each case. This vector may already have reservations, if for example not every port of the cell contention resolution unit is assigned a port unit or if the transmission to a port unit is to be deliberately prevented for certain reasons.

Within a comparator unit, the ascertainment of the authorization information which is to be transmitted to the port unit respectively connected to the comparator unit takes place while maintaining a predetermined sequence with respect to the port units or the individual bits of the reservation vector.

To provide a fairness balance with regard to the receiving port units, the sequence may be selected at the beginning of a cycle of the determination of the authorization information by the N comparator units from a predetermined number of pseudo-randomly regenerated sequences.

Instead of changing the processing sequence within the comparator units after each cycle or a certain number of cycles, each comparator unit can always ascertain the authorization information for the port unit concerned in the sequence of the bits of the

reservation vector. Each comparator unit may then be preceded by a permutation unit, to which the availability vector can be fed and which re-orders the bits of the availability vector in their sequence in accordance with a predetermined specification. Each comparator unit can then similarly be followed by an inverse permutation unit, which, taking into account the performed permutation of the sequence of the bits of the availability vector, ascertains from the information fed to it by the comparator unit, concerning whether and which position of the reservation vector has been reserved, which authorization information is to be transmitted to the port unit connected to the respective comparator unit.

According to one embodiment of the invention, the selection authorization for the transmission of the respective packet or the respective cell to another port unit, respectively, can be checked in each comparator unit by N-1 quota counters provided for each of the other N-1 port units, respectively, or by N quota counters provided for each bit of the reservation vector. The counter reading (quota) of a quota counter is incremented or decremented after each selection of the assigned port unit or after each reservation of the associated bit of the reservation vector. After a predetermined counter reading has been reached, the selection authorization for the port unit concerned or the reservation authorization for the bit concerned of the reservation vector is blocked.

In this case, the provision of N counters again represents the more easily feasible possibility, if a permutation of the bits of the availability vector takes place at the same time, since otherwise the information concerning which of the N bits must not in any case be reserved, because this would mean the packet or the cell being sent back to the respectively

sending port unit, would have to be additionally transmitted to the respective comparator unit. Although this would be possible in theory, the switching of signals between different ports of one and the same port unit is preferably controlled within the respective port unit.

However, it would be readily possible to provide only N-1 quota counters within a comparator unit if the processing sequence of the bits of the reservation vector within a comparator unit were to remain constant, since it is then not always necessary or permissible for one and the same bit to be reserved.

According to one embodiment of the invention, the quota counters (21) of a comparator unit (13) may be respectively assigned to a particular bit of the reservation vector (CRres). The control unit (11) may in this case set all the quota counters (21) of all the comparator units (13) which are assigned to a particular bit of the reservation vector (CRres) to an initial value (initial quota) if there no longer exists a comparator unit (13) in which the quota counter (21) concerned still has a quota and at the same time the bit concerned of the permuted availability vector (CRreq*) indicates a packet to be transmitted or a cell to be transmitted.

According to another embodiment of the invention, the quota counters (21) of a comparator unit (13) may be respectively assigned to a particular port unit (3). In this case, the control unit (11) may set all the quota counters (21) of all the comparator units (13) which are assigned to a particular port unit (3) to an initial value (initial quota) if there no longer exists a comparator unit (13) in which the quota counter (21) concerned still has a quota and at the same time a packet or a cell is to be transmitted from the port

unit connected to the comparator unit (13) to the port unit concerned.

In this case, the comparator units (13) may be fed the permutation information, the comparator units (13) permuting the quota counters in their sequence and taking the information as to whether a cell is available for transmission from the permuted availability vectors CRreq*.

If one or more quota counters are assigned a higher initial quota than other quota counters by the control unit, a prioritizing of particular transmission paths or nodes of the switching device can be accomplished in this way.

According to one embodiment of the invention, the comparator units can be respectively produced by using an N-staged priority encoder, each of the N inputs of the priority encoder being connected to the output of an AND element, and a first input of the AND element being fed the corresponding bit of the possibly permuted availability vector, a second input of the AND element being fed the bit concerned of the reservation vector, which lies at the output of the respectively preceding comparator unit, and a third input of the AND element being fed the information of the associated quota counter, which is logical ONE if there is still a selection authorization, and logical ZERO if there is no longer any selection authorization.

The cell contention resolution unit according to the invention may be designed as a separate integrated circuit. Similarly, however, a unit of this type may also be able to be integrated into a central switching device (a crossbar chip) which has N ports for the connection of a maximum of N port units.

Further embodiments of the invention emerge from the subclaims.

The invention is explained in more detail below on the basis of an exemplary embodiment represented in the drawing, in which:

figure 1 shows the schematic architecture of a switching device, with the simultaneous schematic representation of the data flow, with a cell contention resolution unit according to the invention integrated into the crossbar chip;

figure 2 shows the schematic representation of the central switching unit and of a portal unit in figure 1, with the simultaneous representation of the information flow during collision resolution;

figure 3 shows the schematic structure of the data blocks transmitted from the port units to the central switching unit (figure 3a) and from the central switching unit to the port units (figure 3b);

figure 4 shows the schematic structure of the central switching unit in figures 1 and 2;

figure 5 shows the schematic structure of the cell contention resolution unit according to the invention and

figure 6 shows the schematic structure of the key component of a comparator unit in figure 5.

Figure 1 schematically shows the architecture of a switching device 1 according to the invention, which

comprises a total of N port units 3_1 to 3_N and a central switching unit 5. Each of the N port units 3_1 to 3_N has n ports 7_1 to 7_n, to each of which a signal S_{ij} can be fed, where $1 \leq i \leq n$ and $1 \leq j \leq N$. The port units are usually designed in such a way that bidirectional communication is possible at each port. Of course, however, the principle of the present invention can also be applied to systems in which certain ports or all the ports are designed only for unidirectional communication. However, in practice this tends to be rarely the case.

The port units 3 represented in figure 1 are preferably configured as integrated port modules or separate components. The same applies to the central switching unit 5. This achieves a modular structure, which in turn makes simple scaling possible, i.e. adaptation of the switching device to the respectively required number of data lines to be switched.

As represented in figure 1, the port units 3 and the central switching unit 5 are connected via interface units. The interface units provided in the port units 3 are designated here by "CB-IF" (Crossbar Interface) and the interface units provided in the central switching unit 5 are designated by "Port IF" (Port Interface). In this case, a separate interface unit Port IF is provided in the central switching unit 5 for each port unit 3. As can be seen from figure 4 for the central switching unit, each interface unit Port IF and CB-IF can be connected via a Low Voltage Differential Signaling unit (LVDS) to the transmission lines between the port units 3 and the central switching unit 5. This makes it possible to reduce the number of connection lines, it being possible for example for 16-bit-wide data lines to be provided between the interface units Port IF or CB-IF and the LVDS units and 4-bit-wide data lines (in each case differential signals on a total of 8 physical lines) to be provided

between the LVDS units.

The central switching unit 5 assumes the function of a crossbar switch, so that a completely contemporaneous internal data transmission of a maximum of N (crossbar-internal) signals is possible (if full-duplex transmission via LVDS units is provided). The data inputs/outputs of the interface units Port IF are connected to the actual switching matrix (matrix). Furthermore, a Port IF can switch through the switching matrix in the way conveyed to it, so that the desired path from one Port IF to another Port IF within the central switching unit is available for the data transmission. To prevent a plurality of ports 7 of different port units 3 from simultaneously accessing a port 7 of another port unit - this would mean a cell loss or an internal blockage -, a unit 8 for resolving collisions is provided, also referred to hereafter as a contention resolution unit (CR). The CR unit 8 is preferably provided within the central switching unit and is formed together with the latter as an integrated circuit. Since, as can be seen from the following description, the CR unit 8 has to exchange data very quickly between it and the interface units Port IF, the advantage of very short high-speed transmission lines is produced by the integration of the CR unit.

The method according to the invention and the function of the switching device according to the invention is explained in more detail below with reference to the figures.

According to the representation in figure 1, the ports 7_1 to 7_n of the port units 3_1 to 3_N are each fed a signal S_{1j}. The signals are in each case a stream of data packets, which may vary in length.

The data packets of the individual signals S_{1j} are

firstly segmented by the port units 3, i.e. divided into individual cells of constant length. The cells are stored in a buffer memory 9, which may be integrated in the port units 3 or be formed as an external memory. The segmentation is undertaken by a control unit, which is provided in each port unit 3, is not represented in any more detail and organizes the buffer memory 9 in such a way that a separate virtual buffer memory (9a) is produced for each of the other port units 3, respectively, said separate virtual buffer memory containing the cells to be transmitted to the other port units concerned. For this purpose, each port unit 3 or its control unit evaluates the address information of each packet received, and establishes on the basis of this information whether or not the packet or the corresponding cells have to be transmitted to another port unit 3 and assigns the corresponding cells to the respective virtual (9a) memory. The assignment of the cells of a data packet among one another can be maintained by the provision of pointers. Of course, a separate memory may also be respectively provided for each of the other port units.

The separate or virtual memories (9a) are of the FIFO memory type, since the sequence of the cells must be retained when they are read in and out.

If the port unit establishes that no transmission to another port unit is required, the port unit undertakes the internal switching process within the port unit. Of course, a buffering of the data packets will generally also be necessary for this, but they will not necessarily have to be segmented. Since this port-unit-internal switching function of the switching device 1 is not relevant for the present invention, there is no need for a more detailed explanation.

A buffer memory 9 of this type is necessary for each

port unit 3 in any case, since only one cell of a port unit at a time can be internally transmitted to the central switching unit. Moreover, in the case of an asynchronous transmission of the signals S_{ij}, buffering is necessary to compensate for transmission peaks. This is the case for example in ATM and Ethernet systems, since different services and different ports operate at different data transmission rates and, in particular in the case of IP traffic, the header evaluation time varies greatly.

In principle, it is also possible to dispense with segmentation of the packets for the internal transmission and possible for the data packets as a whole to be transmitted within the switching device 1. However, segmentation produces the advantage that a clock-synchronous transmission can take place within the switching device independently of the respective length of the packets. Moreover, fair handling of the individual (outputs of the) port units is easier.

The transmission of the cells within the switching device 1 takes place clock-synchronously, i.e. one or more cells of the port units 3 are respectively transmitted in a time slot from the port units 3 to the central switching unit 5, and vice versa. In the case of an internal transmission speed of 2 Gbits/s (on each connection between the port units and the central switching unit and within the central switching unit) and a cell length or size of 70 bits, a time slot may have, for example, a time duration of 280 ns.

To avoid a blockage within the switching device, each port unit 3 firstly transmits availability information to the central switching unit 5. The availability information comprises information concerning for which other port units there are at that instant cells for transmission in the respective port unit. Expressed in

the model specified above of the virtual separate buffer memories (9a) provided in the port units for the other port units, respectively, the availability information thus comprises information on whether there is in each case no cell or at least one cell contained in the individual virtual buffer memories.

As represented in figure 3a, the availability information can be transmitted in the header of the cells respectively transmitted from the port units 3 to the central switching unit 5, in order to avoid a separate transmission step and the associated higher protocol complexity.

The availability information may in this case be summarized as a contention request factor (CRreq), the vector comprising N bits in accordance with the number of port units. The position of each bit within the CRreq vector indicates the number j ($1 \leq j \leq N$) of the port unit 3_j and the reservation of the bit concerned indicating whether a cell is available for transmission in the respective port unit for the port unit 3_j.

The CRreq vector does not necessarily have to be linked with the cell actually to be transmitted in the next time slot, but instead may be planned for one or more time slots ahead in the future. In other words, the respective availability information relates to cells which are possibly only transmitted in two or more time slots in the future, it being necessary for this time shift to be constant in the case of all the port units 3.

After receiving the cells, possibly a plurality of cells transmitted simultaneously from the port units, the central switching unit 5 or the interface units Port IF in each case read out the availability information contained therein and transmit it together

with the information concerning from which port unit the availability information was transmitted to the CR unit 8. The CR unit 8 ascertains on the basis of a predetermined contention resolution algorithm in each case a possible combination of permissible, i.e. collision-free, transmission possibilities of corresponding sending port units to corresponding receiving port units.

The combination ascertained in this way is transmitted in the form of authorization information CRgnt at least to those port units 3 which are to receive transmission authorization for the time slot concerned.

As can be seen from figure 3b, this authorization information is preferably in turn transmitted in the header of cells. For example, the respective interface unit Port IF can write in the header of a cell to be transmitted the coded chip ID of the port unit to which a transmission of the port unit connected to the respective interface unit Port IF has been approved, if the port unit connected to the respective Port IF is to be granted a transmission authorization (for the cell concerned) for the time slot concerned. If the port unit concerned is not to be granted authorization, the header may contain in the region reserved for the authorization information a defined reservation, which is interpreted by the port units as "no authorization granted".

After receiving a cell, the central switching unit 5 or the interface units Port IF read out not only the availability vector CRreq but also at least that address information (designated in figure 3 by "destination") which is required to ascertain the port unit to which the cell concerned is to be transmitted.

Instead of an address evaluation of this type, each

interface unit Port IF can also use the authorization information fed to it by the CR unit to switch through the switching matrix in the time slot concerned in such a way that the respective cell is still transmitted to the correct port unit in the same time slot.

Since it is not necessary for a CRreq vector to be contained in the header of the cells which are transmitted from the central switching unit 5 to the respective port units 3, this place in the header may be used for the transmission of other information, for example for status information of the port units 3.

After receiving a cell, the authorization information CRgnt is read out in the port units 3 and it is established whether an authorization (corresponding to the availability information sent before to the central switching unit 5) has been granted for the time slot concerned.

The port unit or the corresponding control unit which, after receiving a cell, establishes that authorization information is present prepares the cell concerned, for which availability information has previously been transmitted to the central switching unit, for transmission in the time slot concerned. To this end, the cell concerned is read out from the memory 9 and transmitted to the interface unit CB-IF.

After port unit 3 has received a cell, the control unit of the port unit reads the address information in the header of the cell and assigns the cell to the respective output port or the respective Media Access Control (MAC) (not represented). Moreover, the individual cells are reassembled to form the original data packets in the port unit or the respective MAC of the individual ports and are transmitted to the respective addressee.

After the interface unit CB-IF of a port unit has received a cell and read out and evaluated the authorization information, new availability information CRreq must be ascertained immediately and inserted in the next cell to be transmitted to the central switching unit 5. This operation is extremely time-critical.

Figure 5 shows the schematic internal structure of the contention resolution unit 8, which has a control unit 11 and a cascade of N comparator units 13 (13_1 to 13_N). In the case of the embodiment represented in figure 5, each comparator unit 13 is preceded by a permutation unit 15 (15_1 to 15_N), which units are in each case connected to the interface units Port IF of the central switching unit 5. The permutation units 15 are subjected to a counter 16. The comparators are connected within the cascade via parallel connection lines 17, via which the reservation vector CRres (see below) respectively of a comparator unit can be transmitted to the next comparator unit in each case within the cascade. In the case of the contention resolution unit represented in figure 5, each comparator unit 13 is followed by an inverse permutation unit 19 (19_1 to 19_N). The control unit 11 activates the counter 16 and, moreover, is connected to each of the comparator units 13. In addition, the control unit 11 is connected via connection lines 17 to the first comparator 13_1 of the cascade.

The contention resolution unit represented in figure 5 operates as follows:

In every time slot, the contention resolution unit 8 runs through a complete cycle, within which the authorization information CRgnt for all port units is ascertained in each case and then transmitted via the

interface units Port IF to the respective port units.

The authorization information CRgnt is in this case ascertained in a clock-pulse controlled manner, the clock in the contention resolution unit 8 preferably being the same as the clock in the rest of the central switching unit.

At the beginning of a complete cycle, the contention request vectors CRreq, i.e. the availability vectors of individual port units, are transmitted to the permutation units 15. Stored in each of the permutation units 15 is a certain number of pseudo-randomly generated sequences, of which the same sequence is in each case active in all the permutation units. By subjecting the permutation units 15 to the output of the counter 16, one particular sequence of these sequences is activated in each case. Of course, the order of the sequences in the permutation units may also be fixed, so that the next sequence in each case can be activated by simply supplying an "advancing pulse".

The sequence can in each case be changed after a certain number of complete cycles. In practice, however, a switch to a different sequence is preferably made after each complete cycle.

The permutation unit uses the respectively active sequence to re-order the bits of the CRreq vector correspondingly. This achieves the effect that none of the port units 3 (as receiving port units) is given preference by its position within the reservation vector. The re-ordered CRreq vectors are transferred to the comparator units 13.

The control unit 11 transfers an initial reservation vector CRres to the first comparator unit 13_1. Also

provided in each comparator unit 13 is a quota counter 21 for each bit of the reservation vector (figure 6). Each quota counter establishes how often the bit concerned of the reservation vector has already been selected by the comparator unit 13 concerned. If a predetermined maximum number is exceeded, the authorization for renewed selection of this bit is blocked in the comparator unit.

To this end, the quota counters 21 may be designed for example as backward counters which can be reset by the control unit (by resetting, the counter is set to a predefined fixed value). If a prioritizing of a port unit (as a sending port unit) is to be deliberately created, the quota counters may be designed as counters which can be loaded with predetermined values by the control unit.

The quota counters preferably have a binary output, with one logical state (for example logical ONE) signaling selection authorization and the other state, respectively, (for example logical ZERO) signaling the absence of selection authorization.

It is firstly checked in the first comparator unit 13_1, on the basis of the initial reservation vector, the re-ordered CRreq vector and the outputs of the quota counters, for each bit of the reservation vector whether the bit is already reserved or is still free. In this case, the initial reservation vector may also have already reserved bits. For example, the control unit may pre-reserve corresponding bits if not all the interface units Port IF of the central switching unit 5 are connected to port units 3.

If a bit is found to be reserved, no further checking is required. If, on the other hand, a bit is detected as free, it is checked whether the bit concerned (with

the same position) of the re-ordered CRreq vector signals the presence of a cell to be transmitted. If this is the case and if a selection authorization is detected on the basis of the output of the quota counter concerned, the comparator unit 13_1 reserves the bit concerned of the reservation vector. This concludes the checking operation, since only one cell at a time can be transmitted to the corresponding port unit. If the absence of selection authorization is detected for this bit of the reservation vector CRres or if the CRreq vector indicates no cell to be transmitted, the checking operation is continued. This checking procedure is carried out until a bit of the CRres vector has been reserved by the comparator unit 13_1 or until all the bits of the vector have been checked.

In the case of the embodiment represented in figure 5, this checking is preferably performed in the sequence of the bits of the CRres vector.

In principle, however, it would also be possible, instead of the re-ordering of the CRreq vectors in the permutation units 15, to change the checking sequence of the bits of the CRres vector in the comparator units.

After the CRres vector has been checked in the comparator unit 13_1, it is transferred to the comparator unit 13_2. Then a checking operation proceeds again in this unit in the same way as explained above. These steps are repeated until the reservation vector has been checked by all the comparator units and any corresponding free bits have been reserved. This concludes the complete cycle.

At the end of each complete cycle, the authorization information present at the output of each inverse

permutation unit 19 is transmitted via the respective interface unit Port IF to the port unit 3 concerned. Each inverse permutation unit 19 receives from the comparator unit 13 concerned the information as to whether a bit, and which bit, of the reservation vector has been reserved. The inverse permutation unit knows the re-ordering specification used by the permutation units and ascertains from the bit position which has been reserved the original bit position again.

To this end, inverse sequences can be stored in the inverse permutation units 19 and can be used to reverse the re-ordering performed in the permutation units 15. As in the case of the permutation units 15, it is also possible in the case of the inverse permutation units 19 to bring about a selection or advancement of the inverse sequences by the output of the counter 13 supplied to them.

In addition, after switching back the respective reservation vector CRres and the assignment known to it of the port units 3 to the positions of the CRreq vector, each inverse permutation unit 19 can transmit to the port unit connected to the respective comparator unit, as authorization information CRgnt, the ID number of that port unit 3 to which the last-mentioned one cell can be transmitted.

Before the beginning of the check on the CRres vector in the cascade of the comparator units 13 (or after ending of the check on the CRres vector in the preceding complete cycle), the control unit 11 establishes whether at least one quota counter 21 of a comparator unit 13 still has a quota for a particular bit within the CRres vector and at the same time the bit concerned of the permuted CRreq vector fed to this comparator unit (designated by CRreq*) indicates a cell to be transmitted to the port unit 3 concerned. If

this is not the case, the control unit 11 instigates a resetting of all the quota counters 21, responsible for the bit concerned of the CRres vector, of the comparator units 13 to the initial quota.

While in the case of the option described above the quota counters 21 were assigned in a simple way to one particular bit of the CRres vector, in another embodiment the quota counters 21 may be assigned to the outputs of the central switching unit 5 or to the port units. Since, however, the comparators 13 are in any case fed the permuted vectors CRreq*, in this case the comparator units 13 must also be conveyed the permutation information. With this information it is then possible, for the check as to whether certain counters must be set to an initial quota, either to carry out a re-ordering also of the sequence of the quota counters or to reverse the re-ordering of the bits of the CRreq* vectors.

According to another embodiment, it is also possible to transmit the non-permuted CRreq vectors to the comparator units 13 in addition to the CRreq* vectors. Consequently, the quota counters 21 assigned to the port units 2 can establish directly whether a cell still has to be transmitted to the port unit 3 concerned.

If dispensing with a prioritizing of the respectively sending port units 3, in the simplest case the quota one can be used, it being possible here for the quota counters to take the form of a bit, produced in terms of technical hardware, for example, by a flipflop. The quota counters can then also be combined to form a vector with N bits and be produced for example by a register of the length N. A set bit can then indicate for example an existent quota and a non-set bit can indicate an absent quota.

Figure 6 shows the basic structure of the key component of an embodiment of a comparator unit 13. This comprises an N-staged priority encoder 23, the behavior of which can be described as follows: each output O_i ($1 \leq i \leq N$) is set to logical ONE if all the previous inputs I_{i-1} are at logical ZERO and the associated input I_i is at logical ONE. In other words, only that output for which the associated input in the sequence of the N stages of the priority encoder is the first that lies at logical ONE is set to logical ONE.

Figure 6 shows in this respect only the first four stages A, B, C, D of the priority encoder 23 with the input states a, b, c, d and logic connections which produce the corresponding output states.

The inputs I_i of the individual stages of the priority encoder 23 are in each case connected to the output of an AND gate 25, which in each case logically links three signals by an AND operation, that is the respective bit CRreq[i] of the CRreq vector, the respective bit CRres[i] of the reservation vector CRres, fed to the comparator unit 13, and the output of the respective quota counter 21. This achieves the desired aim of reserving the respective bit of the reservation vector only if it was still unreserved and if a corresponding cell is to be transmitted, and at the same time there is a reservation authorization.

For the starting of a contention resolution cycle, the control unit 11 may receive a start pulse CR_{start}. The checking of the reservation authorization, possibly including the generation of the authorization information CRgnt, may take place in a clock-pulse controlled manner, to ensure dependability. In this case, for example, only the actions required in one comparator unit 13 in each case are carried out in a

clock cycle. The respectively processed CRres vector can then be transferred by means of an output register (not represented) to the next comparator unit respectively of the cascade.

If the switching times of the individual components, the signal transit times, etc. allow, a plurality of comparator units 13 may also be combined. To this end, in the embodiment according to figure 6, the outputs of the priority encoder 23 of a comparator unit 13 are respectively connected directly to the inputs, for example the inputs concerned of the AND gates 25. This measure allows the actions of a plurality of comparator units, or even all the comparator units, to be executed within one clock cycle, as a result of which an enormous increase in processing speed can be achieved.

Patent claims

1. A cell contention resolution unit for a device for switching a plurality of packet-oriented signals,

a) the switching device (1) comprising a central switching unit (5) and a maximum of N port units (3) connected to the latter and each having n ports (7), to each of which a signal can be fed,

b) the cell contention resolution unit (8) having N inputs, to each of which an availability vector (CRreq) with availability information can be fed by one of the N port units (3), comprising information on whether, and to which further port units (3), a packet of a signal or a cell of a segmented packet of a signal is to be transmitted,

c) each availability vector (CRreq) being able in each case to be fed to a comparator unit (13) of a cascade of N comparator units (13_1 to 13_N), which are connected to a control unit (11), and

d) each comparator unit (13) using the respective availability vector (CRreq), reservation information (CRres) generated by the respectively preceding comparator (13) or the control unit (11) with respect to the transmission of the respective packet or the respective cell to the port units and using selection authorization information for the transmission of the respective packet or the respective cell to the port units (3) to ascertain authorization information (CRgnt) and transmit it to the port unit (3) connected to it, comprising information concerning to which other port unit (3) the port unit (3) connected

to the respective comparator unit (13) is authorized for the transmission of a corresponding packet or a corresponding cell, whereby altogether a blockage-free combination of packets or cells which can be transmitted simultaneously between the port units (3) is ascertained,

e) the reservation information (CRres) generated by a comparator unit (13) in each case being transferred in parallel in the form of a reservation vector (CRres) to the next comparator unit (13) respectively and processed in the comparator units in parallel or semi-parallel.

2. The cell contention resolution unit as claimed in claim 1, in which the processing of the reservation vector (CRres) in the comparator units (13) and the transfer of the reservation vector (CRres) between the comparator units (13) takes place in a clock-pulse controlled manner, the reservation vector (CRres) being processed in at least one comparator unit (13) and prepared for transfer to the respectively following comparator unit (13) in each clock cycle.

3. The cell contention resolution unit as claimed in claim 2, in which the reservation vector (CRres) is processed in a plurality of comparator units (13) or all the comparator units (13) in each clock cycle.

4. The cell contention resolution unit as claimed in one of the preceding claims, in which each availability vector (CRreq) has N bits, the position of a bit in the availability vector (CRreq) comprising the assignment of the

information contained in this bit to a particular port unit (3), and the one logical state of the bit signaling the availability of a packet or a cell intended for the port unit (3) concerned and the other logical state, respectively, signaling the absence of the availability of a packet or a cell.

5. The cell contention resolution unit as claimed in one of the preceding claims, in which the reservation vector (CRres) has N bits, the position of a bit in the reservation vector (CRres) comprising the assignment of the information contained in this bit to a particular receiving port unit (3), and the one logical state of the bit signaling the already performed reservation of the port unit (3) concerned for the reception of a packet or a cell from another port unit (3), and the other logical state, respectively, signaling the readiness of the port unit concerned.

6. The cell contention resolution unit as claimed in claim 5, in which the control unit (11) transfers an initial reservation vector (CRres) to the first comparator unit (13_1) of the cascade of N comparator units (13).

7. The cell contention resolution unit as claimed in claim 6, in which those bits of the reservation vector (CRres) which correspond to port units (3) which are not available for reception or not present are pre-reserved with the corresponding logical state.

8. The cell contention resolution unit as claimed in one of the preceding claims, in which each comparator unit (13) ascertains the authorization information for the port unit (3) concerned in a predetermined sequence with respect to the port

units (3) or the individual bits of the reservation vector (CRres).

9. The cell contention resolution unit as claimed in claim 8, in which the sequence is selected at the beginning of a cycle of the determination of the authorization information (CRgnt) by the N comparator units (13) from a predetermined number of pseudo-randomly generated sequences.

10. The cell contention resolution unit as claimed in one of claims 1 to 8, in which each comparator unit (13) ascertains a possible reservation of bits of the reservation vector (CRres) in the sequence of the bits of the reservation vector (CRres), in which each comparator unit (13) is preceded by a permutation unit (15), to which the availability vector (CRreq) can be fed and which re-orders the bits of the availability vector (CRreq) in their sequence in accordance with a predetermined specification and in which each comparator unit (13) is followed by an inverse permutation unit (19), which, taking into account the performed permutation of the sequence of the bits of the availability vector (CRreq), ascertains from the information fed to it by the comparator unit (13), concerning whether and which position of the reservation vector (CRres) has been reserved, which authorization information (CRgnt) is to be transmitted to the port unit (3) connected to the comparator unit (13) concerned.

11. The cell contention resolution unit as claimed in one of the preceding claims, in which the selection authorization for the transmission of the respective packet or the respective cell to another port unit (3), respectively, is provided in each comparator unit (13) by N-1 quota counters (21)

provided for each of the other N-1 port units (3), respectively, or by N quota counters (21) provided for each bit of the reservation vector (CRres), the counter reading (quota) of a quota counter (21) being incremented or decremented after each selection of the assigned port unit (3) or after each reservation of the associated bit of the reservation vector (CRres) and, once a predetermined counter reading has been reached, the selection authorization for the port unit (3) concerned or the reservation authorization for the bit concerned of the reservation vector (CRres) being blocked.

12. The cell contention resolution unit as claimed in claim 11, in which the quota counters (21) of a comparator unit (13) are respectively assigned to a particular bit of the reservation vector (CRres) and in which the control unit 11 sets all the quota counters (21) of all the comparator units (13) which are assigned to a particular bit of the reservation vector (CRres) to an initial value (initial quota) if there no longer exists a comparator unit (13) in which the quota counter (21) concerned still has a quota and at the same time the bit concerned of the permuted availability vector (CRreq*) indicates a packet to be transmitted or a cell to be transmitted.

13. The cell contention resolution unit as claimed in claim 11, in which the quota counters (21) of a comparator unit (13) are respectively assigned to a particular port unit (3) and in which the control unit (11) sets all the quota counters (21) of all the comparator units (13) which are assigned to a particular port unit (3) to an initial value (initial quota) if there no longer exists a comparator unit (13) in which the quota counter

(21) concerned still has a quota and at the same time a packet or a cell is to be transmitted from the port unit connected to the comparator unit (13) to the port unit concerned.

14. The cell contention resolution unit as claimed in claim 13, in which the comparator units (13) are fed the permutation information, in which the comparator units (13) permute the quota counters and take the information as to whether a cell is available for transmission from the permuted availability vectors CRreq*.

15. The cell contention resolution unit as claimed in one of claims 12 to 14, in which one or more quota counters (21) are assigned a higher initial quota than other quota counters (21).

16. The cell contention resolution unit as claimed in one of the preceding claims, in which the comparator units (13) each have an N-staged priority encoder (23), each of the N inputs (I_1 to I_N) of the priority encoder (23) being connected to the output of an AND element (25), and a first input of the AND element being fed the corresponding bit (CRreq[i]) of the availability vector or of the permuted availability vector (CRreq*[i]), a second input of the AND element (25) being fed the bit concerned of the reservation vector (CRres[i]), which lies at the output of the respectively preceding comparator unit (13), and a third input of the AND element (25) being fed the information of the associated quota counter (21), which is logical ONE if there is still a selection authorization, and logical ZERO if there is no longer any selection authorization.

17. The cell contention resolution unit as claimed in

one of the preceding claims, which is designed as an integrated circuit.

18. A central switching device with N ports for the connection of a maximum of N port units (3), which is designed as an integrated circuit which comprises a cell contention resolution unit (8) as claimed in one of claims 1 to 14.

S0258

Abstract

Cell contention resolution unit for a device for switching a plurality of packet-oriented signals

For contention resolution, a reservation vector is pushed through a cascade of comparator units in the contention resolution unit, each comparator unit evaluating a contention request vector fed to it and in each case reserving only the first possible bit of the reservation vector. A minimum fairness balance is achieved by a quota control. The parallel or semi-parallel processing of the reservation vector in the cascade produces an extremely high processing speed.

S0258

List of designations

1	switching device
3	port unit (3_1 to 3_N)
5	central switching unit
7	ports of the port units (7_1 to 7_n)
8	unit for resolving collisions (contention resolution unit)
9	buffer memory
9a	virtual buffer memory
11	control unit
13	comparator unit (13_1 to 13_N)
15	permutation unit (15_1 to 15_N)
16	counter
17	connection lines
19	inverse permutation unit (19_1 to 19_N)
21	quota counter
23	priority encoder
25	AND gate
a,b,c,d	logical states
A,B,C,D	stages 1 to 4 of the priority encoder
I_i, O_i	inputs and outputs of the priority encoder ($1 \leq i \leq N$)
CRgnt	authorization information
CRreq	contention request vector, availability information
CRres	reservation vector
CR_{start}	start signal for contention resolution cycle
N	number of port units
Port IF	interface units in 5
CB-IF	interface units in 3
LVDS	Low Voltage Differential Signaling
S_{ij}	signals to the ports 7 (indices i, j)

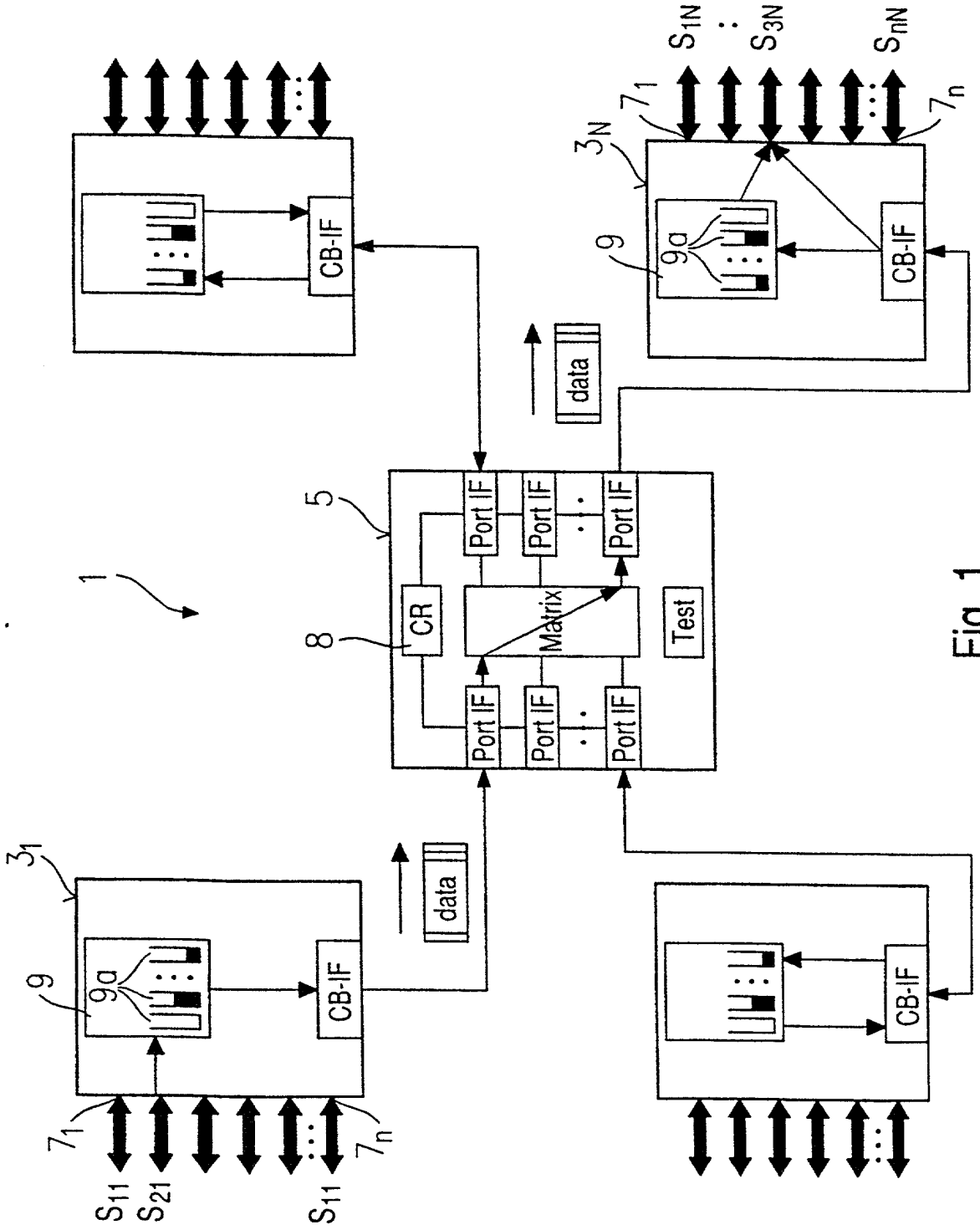
1
5
8
9
9a
3_1
3_N
7_1
7_n
S_{11}
S_{21}
S_{1N}
S_{3N}
S_{nN}
CB-IF
Port IF
CR
Matrix
Test
data

Fig. 1

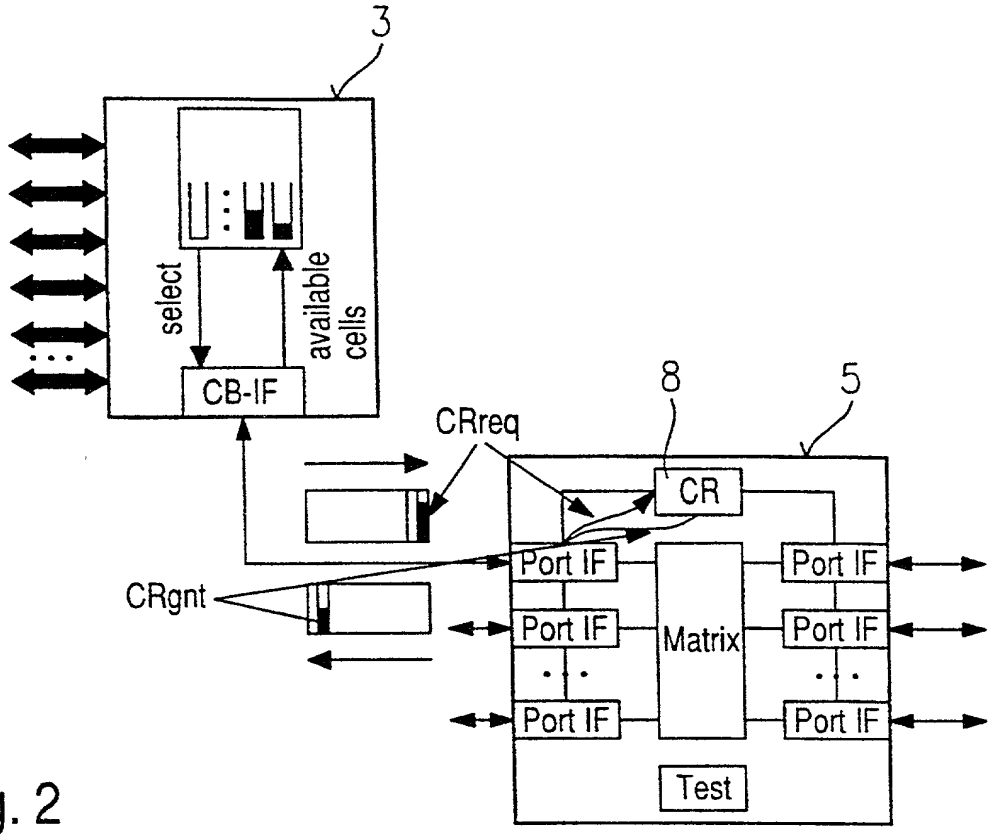

Fig. 2

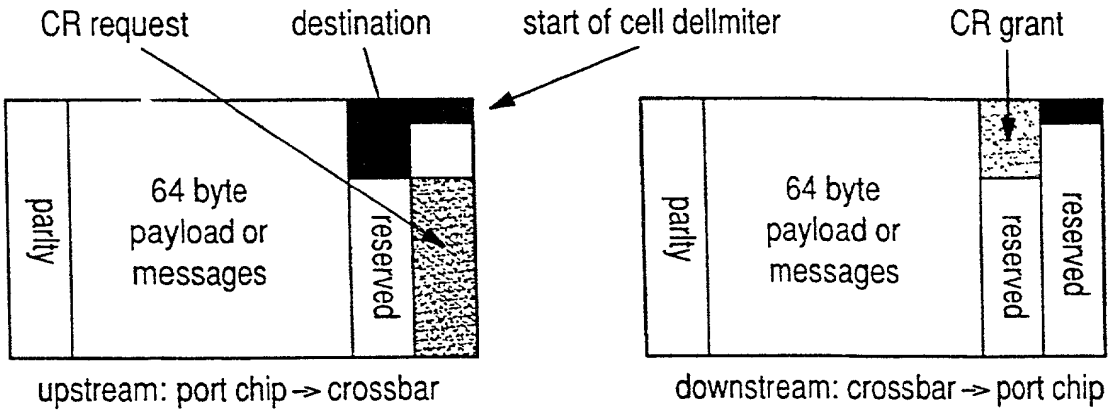

Fig. 3a

Fig. 3b

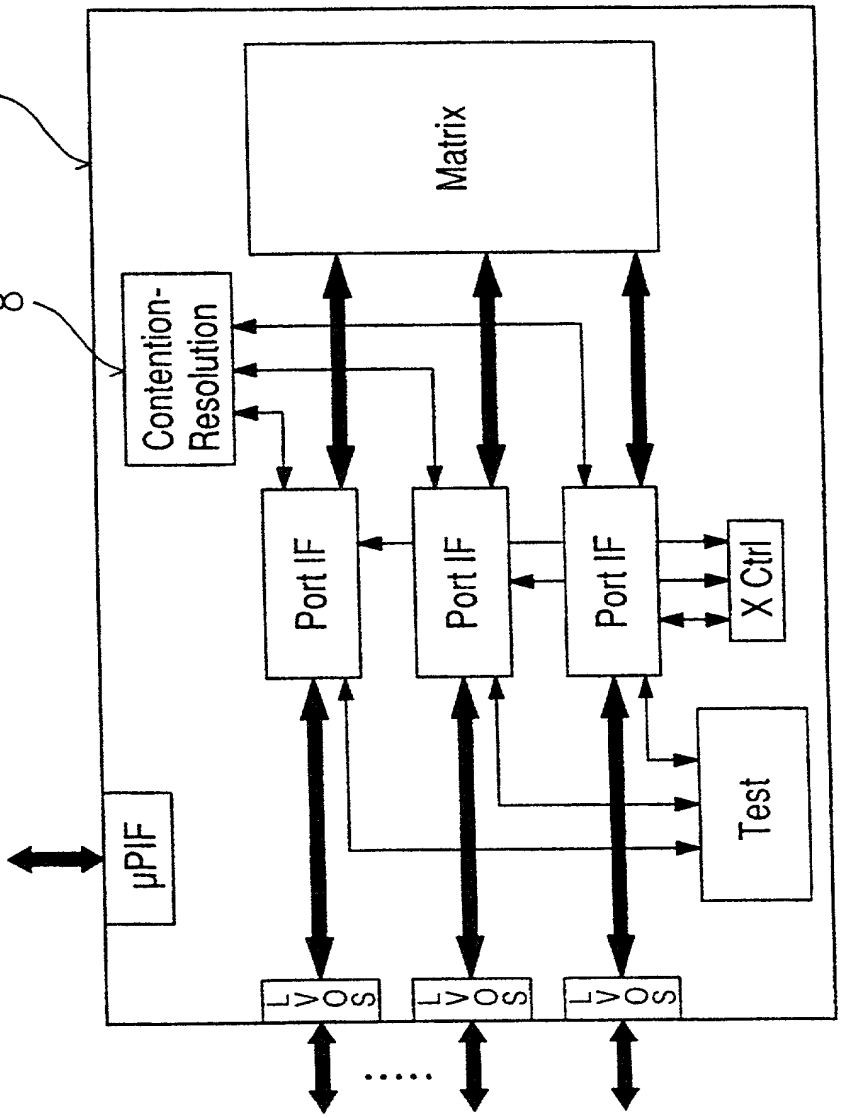
5
Matrix
8
Contention-Resolution
Port IF
Port IF
Port IF
X Ctrl
Test
µPIF
LVDS
LVDS
LVDS

Fig. 4

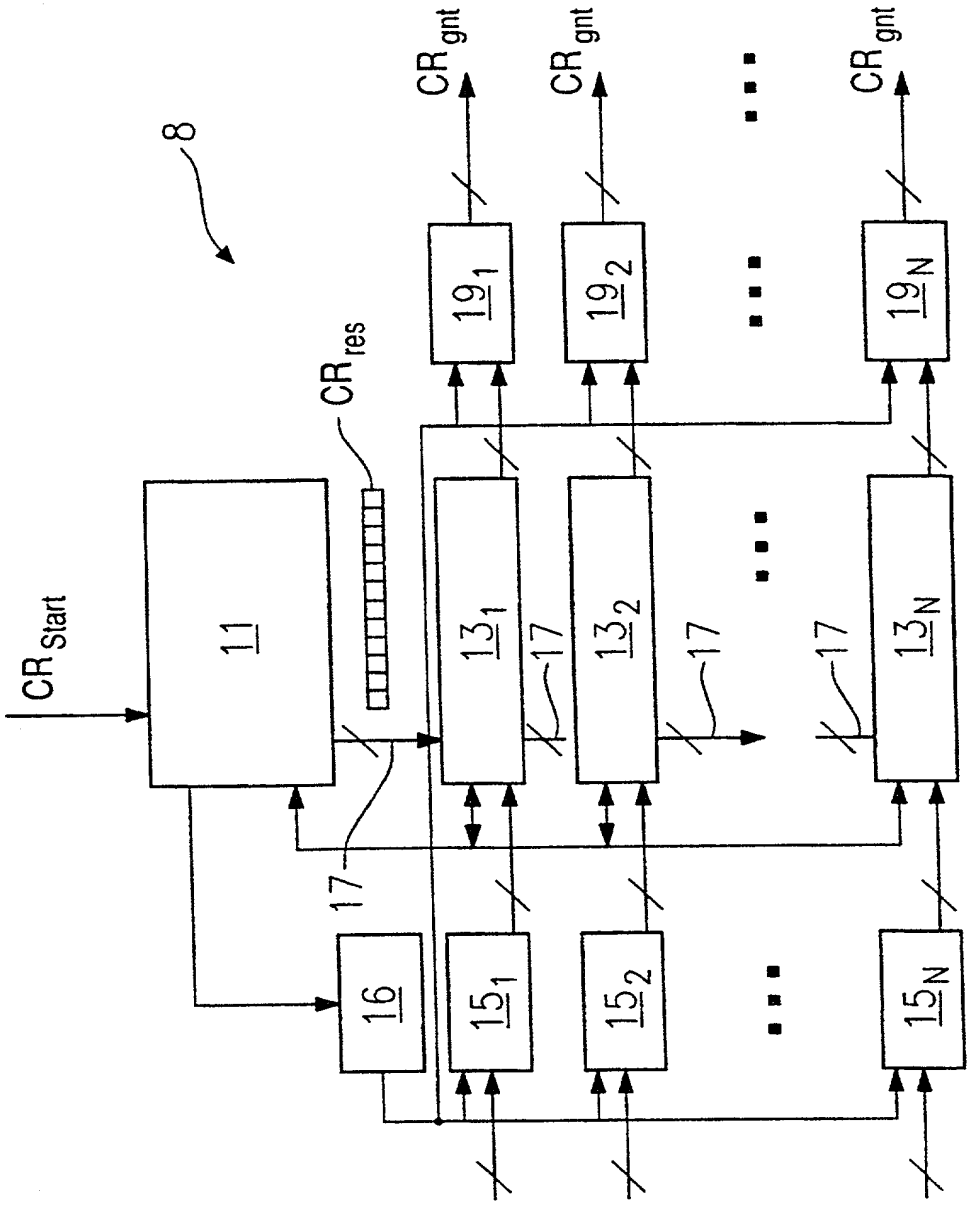
8
CR Start
11
CR res
17
13 1
13 2
13 N
19 1
19 2
19 N
CR gnt
CR gnt
CR gnt
16
15 1
15 2
15 N

Fig. 5

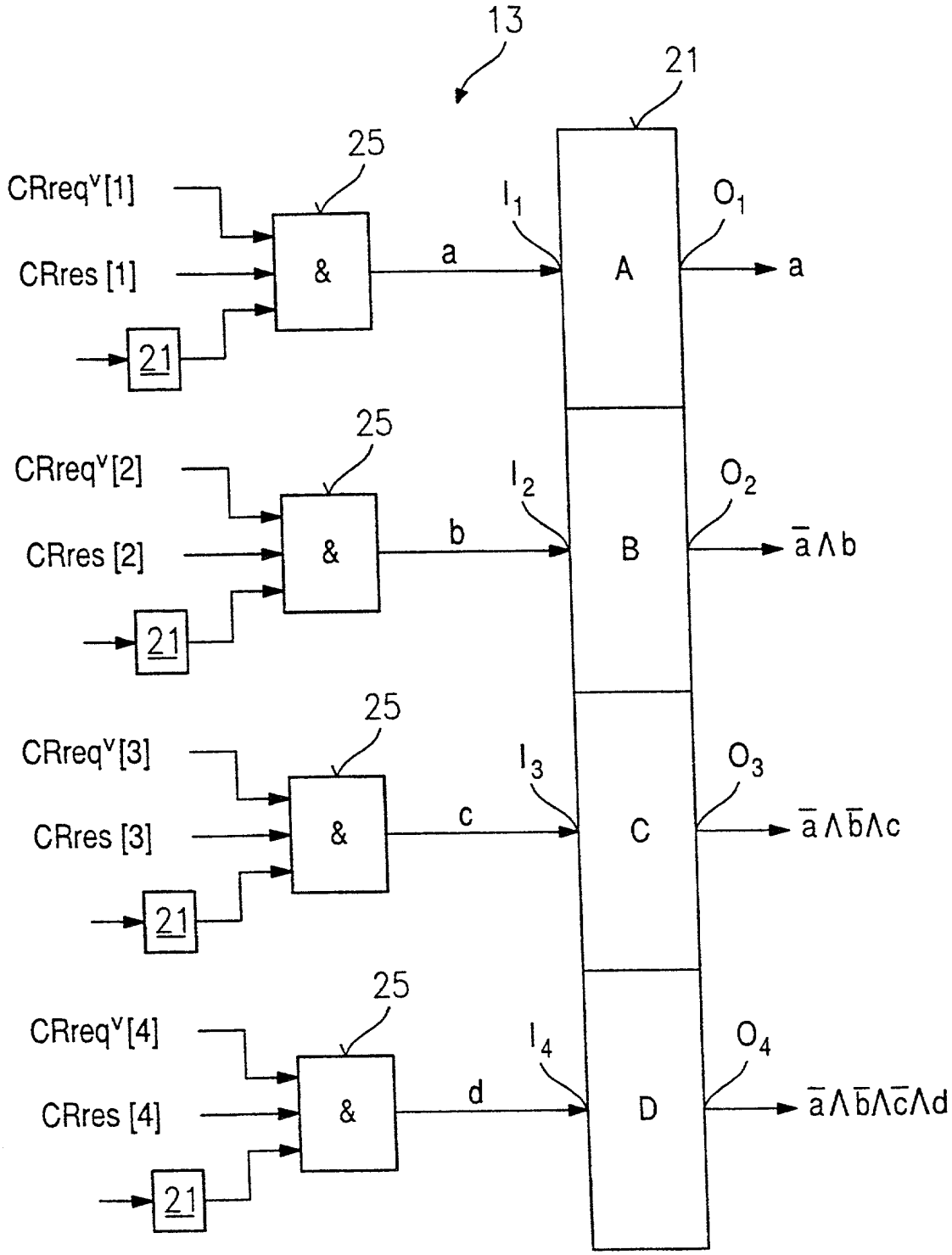
13
21
25
CRreq^{v}[1]
CRres [1]
21
&
a
I_1
A
O_1
a
25
CRreq^{v}[2]
CRres [2]
21
&
b
I_2
B
O_2
$\bar{a} \wedge b$
25
CRreq^{v}[3]
CRres [3]
21
&
c
I_3
C
O_3
$\bar{a} \wedge \bar{b} \wedge c$
25
CRreq^{v}[4]
CRres [4]
21
&
d
I_4
D
O_4
$\bar{a} \wedge \bar{b} \wedge \bar{c} \wedge d$

Fig. 6

TO/SB/01 (6/95) DECLARATION Docket No. 8074-5 (S1595 SB/fis)

S1595

AS A BELOW NAMED INVENTOR, I hereby declare that:

My residence, post office address and citizenship are as stated next to my name.

I believe that I am the original, first and sole *(if only one name is listed below)*, or an original, first and joint inventor *(if plural names are listed below)*, of the subject matter which is claimed and for which a patent is sought on the invention entitled:

TITLE: CELL CONTENTION RESOLUTION UNIT FOR A DEVICE FOR SWITCHING A PLURALITY OF PACKET-ORIENTED SIGNALS

the specification of which either is attached hereto or indicates an attorney docket no. 8074-5 (S1595 SB/fis), or:

☐ was filed in the U.S. Patent & Trademark Office on _____ and assigned Serial No. _____,

☐ and *(if applicable)* was amended on _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to patentability and to the examination of this application in accordance with Title 37 of the Code of Federal Regulations §1.56. I hereby claim foreign priority benefits under Title 35, U.S. Code §119(a)-(d) or §365(b) of any foreign application(s) for patent or inventor's certificate, or §365(a) of any PCT international application which designated at least one country other than the United States, or §119(e) of any United States provisional application(s), listed below and have also identified below any foreign applications for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

			Priority Claimed:
199 41 851	Germany	02 September 1999	Yes [X] No [ ]
(Application Number)	*(Country)*	*(Day/Month/Year filed)*	
			Yes [ ] No [ ]
(Application Number)	*(Country)*	*(Day/Month/Year filed)*	

☐ I hereby claim the benefit under Title 35, U.S. Code, §120, of any United States application(s), or §365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application(s) in the manner provided by the first paragraph of Title 35, U.S. Code, §112, I acknowledge the duty to disclose information material to patentability as defined in Title 37, The Code of Federal Regulations, §1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial Number)	*(Filing Date)*	*(STATUS: patented, pending, abandoned)*
(Application Serial Number)	*(Filing Date)*	*(STATUS: patented, pending, abandoned)*

I hereby appoint the following attorneys: **FRANK CHAU**, Reg. No. 34,136; **FRANK V. DeROSA**, Reg. No. 43,584; **GASPARE J. RANDAZZO**, Reg. No. 41,528; **SUSAN PAIK**, Reg. No. 46,347; **JUAN C. VILLAR**, Reg. No. 34,271; **NATHANIEL T. WALLACE**, Reg. No. 48,909; and **ERIC M. PARHAM**, Reg. No. 45,747, each of them of **F. CHAU & ASSOCIATES, LLP**, 1900 Hempstead Turnpike, Suite 501, East Meadow, New York, 11554, to prosecute this application and to transact all business in the U.S. Patent and Trademark Office connected therewith and with any divisional, continuation, continuation-in-part, reissue or re-examination application, with full power of appointment and with full power to substitute an associate attorney or agent, and to receive all patents which may issue thereon, and request that all correspondence be addressed to:

Frank Chau, Esq.
F. CHAU & ASSOCIATES, LLP
1900 Hempstead Turnpike, Suite 501
East Meadow, New York 11554
Tel. No.: (516) 357-0091

HEREBY DECLARE that all statements made herein of my own knowledge are true and that all statements made n information and belief are believed to be true; and further that these statements were made with the knowledge that Willful false statements and the like so made are punishable by fine or imprisonment, or both, under §1001 of Title 18 J.S. Code and that such willful false statements may jeopardize the validity of the application or any patent issued hereon.

1 - 00

ULL NAME OF FIRST OR SOLE INVENTOR: Mathias Hellwig Citizenship Germany

nventor's signature: _____ Date: 18.02.02

Residence & Post Office Address: 1 Regal Court
North Brunswick, New Jersey 08902 NJ

ULL NAME OF SECOND JOINT INVENTOR: Andreas Kirstaedter Citizenship Germany

nventor's signature: _____ Date: _____

Residence & Post Office Address: Raiffeisenstr. 6
D-85560 Ebersberg
Germany

ULL NAME OF THIRD JOINT INVENTOR: _____ Citizenship _____

nventor's signature: _____ Date: _____

Residence & Post Office Address:

ULL NAME OF FOURTH JOINT INVENTOR: _____ Citizenship _____

nventor's signature: _____ Date: _____

Residence & Post Office Address:

ULL NAME OF FIFTH JOINT INVENTOR: _____ Citizenship _____

nventor's signature: _____ Date: _____

Residence & Post Office Address:

ULL NAME OF SIXTH JOINT INVENTOR: _____ Citizenship _____

nventor's signature: _____ Date: _____

Residence & Post Office Address:

HEREBY DECLARE that all statements made herein of my own knowledge are true and that all statements made information and belief are believed to be true; and further that these statements were made with the knowledge that illful false statements and the like so made are punishable by fine or imprisonment, or both, under §1001 of Title 18 .S. Code and that such willful false statements may jeopardize the validity of the application or any patent issued hereon.

FULL NAME OF FIRST OR SOLE INVENTOR: Mathias Hellwig Citizenship Germany

Inventor's signature: _____ Date: _____
Residence & Post Office Address: 1 Regal Court
North Brunswick, New Jersey 08902

2-00
FULL NAME OF SECOND JOINT INVENTOR: Andreas Kirstaedter Citizenship Germany

Inventor's signature: A. Kirstädter Date: 14.2.02
Residence & Post Office Address: Raiffeisenstr. 6
D-85560 Ebersberg DEX
Germany

FULL NAME OF THIRD JOINT INVENTOR: _____ Citizenship _____

Inventor's signature: _____ Date: _____
Residence & Post Office Address:

FULL NAME OF FOURTH JOINT INVENTOR: _____ Citizenship _____

Inventor's signature: _____ Date: _____
Residence & Post Office Address:

FULL NAME OF FIFTH JOINT INVENTOR: _____ Citizenship _____

Inventor's signature: _____ Date: _____
Residence & Post Office Address:

FULL NAME OF SIXTH JOINT INVENTOR: _____ Citizenship _____

Inventor's signature: _____ Date: _____
Residence & Post Office Address: